

Remarks/Arguments

The specification has been amended to address the objections to the drawings and specification as identified by the examiner. It is submitted that these objections have been overcome through the amendments.

35 U.S.C. §102

Claims 1-5, 11, 12, and 14-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by McNeely, U.S. Patent No. 4,814,879.

Claims 1, 2, 4-6 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kuwata et al., U.S. Patent App. No. 2004/0062336.

Claims 1-4, 6, 11, 14 and 15 stand rejected under 35 U.S.C. §102(a) as being anticipated by Ito, U.S. Patent App. No. 2003/0117190.

It is submitted that McNeely does not teach or suggest

“an analog to digital converter for generating a digital signal in response to a first clock signal;
a fixed rate clock generator for generating said first clock signal;
a phased lock loop for generating a second clock signal in response to said first clock signal;
a delay means comprising a plurality of outputs for delaying the first clock signal responsive to the second clock signal;
a means to compare said plurality of outputs of the delay means to produce a first output signal wherein the first output signal produced is a synchronization of the first clock signal and the second clock signal; and
a processing means to process said digital signal in response to said first output signal”

as recited by the currently amended claim 1.

The present invention teaches a system comprising an A/D converter operating in response to a fixed rate clock, a PLL for generating a second clock signal in response to the fixed rate

clock, and then a system for comparing and synchronizing the first clock signal to the second clock signal and producing an output signal used to process the digital signal.

McNeely teaches a system for aligning a transition of a clock signal to the transitions of a horizontal line sync signal. (abstract) McNeely does not teach or suggest generating a digital signal in response to a fixed rate clock signal, then synchronizing the fixed rate clock signal to a second clock signal generated by a PLL, and then using the resulting output signal to process the digital signal. McNeely merely teaches a system of aligning the transitions of two signals to generate a clock signal. Since McNeely does not teach or suggest “an analog to digital converter for generating a digital signal in response to a first clock signal” or “a phased lock loop for generating a second clock signal in response to said first clock signal” it is submitted that currently amended claim 1 is allowable over McNeely. Such action is respectfully requested. Furthermore, it is submitted that claims 4-6 and 11-16 are allowable for at least the same reasons that claim 1 is allowable. Such action is respectfully requested.

It is submitted that Kuwata et al., teaches a timing extraction circuit which uses a PLL to generate a clock signal for extracting a clock signal from a data signal. (abstract) Kuwata et al., does not teach or suggest generating a digital signal in response to a fixed rate clock signal, then synchronizing the fixed rate clock signal to a second clock signal generated by a PLL, and then using the resulting output signal to process the digital signal. McNeely merely teaches a system of aligning the transitions of two signals. One with a frequency of $\frac{1}{2}$ the other, to generate a clock signal. Since Kuwata et al., does not teach or suggest “an analog to digital converter for generating a digital signal in response to a first clock signal” or “a phased lock loop for generating a second clock signal in response to said first clock signal” it is submitted that currently amended claim 1 is allowable over Kuwata et al. Such action is respectfully requested. Furthermore, it is submitted that claims 4-6 and 11-16 are allowable for at least the same reasons that claim 1 is allowable. Such action is respectfully requested.

It is submitted that Ito et al., teaches a system for aligning the phase response of two clock signals. (abstract) Ito does this by detecting the phase difference between the first and second clock and uses variable delay lines to advance or delay one or both of the input clocks before they are input into a PLL where they are synchronized. (Col. 4, lines 15-45) Ito does not teach or suggest generating a digital signal in response to a fixed rate clock signal, then synchronizing the fixed rate clock signal to a second clock signal generated by a PLL, and then using the resulting output signal to process the digital signal. Ito merely

teaches a system of aligning two signals to generate a clock signal by delaying the clock signals to a sufficient degree that a PLL operation can be performed. Since Ito does not teach or suggest “an analog to digital converter for generating a digital signal in response to a first clock signal” or “a phased lock loop for generating a second clock signal in response to said first clock signal” it is submitted that currently amended claim 1 is allowable over Ito. Such action is respectfully requested. Furthermore, it is submitted that claims 4-6 and 11-16 are allowable for at least the same reasons that claim 1 is allowable. Such action is respectfully requested.

35 U.S.C. §103

Claims 12 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ito, U.S. Patent App. No. 2003/0117190 in view of Renner et al., U.S. Patent App. No. 2005/0007493. Since claim 11 is allowable and claims 12 and 13 are dependent on claim 11, it is submitted that claims 12 and 13 are allowable for at least the same reasons that claim 11 is allowable. Such action is respectfully requested.

Having fully addressed the Examiner’s rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant’s representative at (609) 734-6804, so that a mutually convenient date and time for a telephonic interview may be scheduled. No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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